REMARKS

Claims 1-27 are currently pending in the present patent application.

In the Office Action, the Examiner allowed claim 14-27 and objected to claims 8-12 as depending upon a rejected base claim but indicated these claims would be allowable if properly rewritten. Claim 8 has been rewritten in independent form and claims 2-7 and 9-13 amended to depend directly or indirectly from claim 8. Accordingly, claims 2-13 are also in condition for allowance. Claims 1, 4, and 14 have also been amended to clarify the recited subject matter based upon the Examiner's objections to these claims. These amendments do not narrow the scopes of any of these claims.

The Examiner rejected claim 1 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent Application Publication No. 2002/0085423 to Tedrow *et al.* ("Tedrow").

The minor amendments to claim 1 merely clarify the recited subject matter and do not narrow the scope of this claim. Amended claim 1 recites, in part, a plurality of volatile memory cells, each volatile memory cell having a capacitive storage element. Each volatile memory cell is associated with a respective access signal line and the capacitive storage element of each volatile memory cell includes the capacitance intrinsically associated with the respective access signal line. Claim 1 expressly recites that the capacitive storage element of each volatile memory cells includes the capacitance intrinsically associated with the corresponding access signal line.

Tedrow neither discloses nor suggests such a structure. While the capacitance of associated access or bit lines may be used in sensing data stored in conventional volatile memory cells, each cell includes a dedicated storage element that is separate from the bit line. Figures 2 and 3 of Tedrow are no different except that these figures are not even concerned with volatile memory cells but instead illustrate a portion of a conventional FLASH memory cell array. Claim 1 recites volatile memory cells, each memory cell having a capacitive storage element that includes the capacitance intrinsically associated with the respective access signal line. In claim 1 the recited structure of each recited volatile memory cell must

necessarily have each cell operate to store data written to the cell and provide data being read from the cell, which is the function of such a memory cell.

Merely saying that bit lines or other lines in a conventional memory-cell array have capacitance and thus could be used as such memory cells is not a sufficient teaching or suggestion in Tedrow or any other reference. Such references are myriad as all conventional memory-cell arrays posses these characteristics. The bit lines in Tedrow simply do not function as the capacitive storage element of a volatile memory cell but are utilized in a conventional manner to transfer data to and from the cells. Of course these lines posses capacitance, but this capacitance is not being used as the storage element of a volatile memory cell as expressly recited in claim 1. For all these reasons, the combination of elements recited in claim 1 is allowable over Tedrow and all of the other references of record, whether taken singly or in combination.

The present patent application is in condition for allowance. Favorable consideration and a Notice of Allowance are respectfully requested. Should the Examiner have any further questions about the application, Applicant respectfully requests the Examiner to contact the undersigned attorney at (425) 455-5575 to resolve the matter. If a need for any fee in addition to that paid with this response is found, for any reason or at any point during the prosecution of this application, kindly consider this a petition therefore and charge any necessary fees to Deposit Account 07-1897.

Dated this 2nd day of August, 2005.

Respectfully submitted,

GRAYBEAL JACKSON HALEY LLP

Paul F. Rusyn
Registration No. 42,118
155 – 108th Avenue NE, Suite 350
Bellevue, WA 98004-5973
(425) 455-5575 Phone
(425) 455-5575 Fax

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